Honeywell

DATA HIWAY INTERFACE MAINTENANCE

ADHI-M
10/13/78

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DATA HIWAY INTERFACE (DHI) MAINTENANCE

1. INTRODUCTION

The repair and maintenance information contained in this section of the computer maintenance manual applies to the Data Hiway Interface (DHI) or the Hiway Interface Module (HIM). These are GENIE* Bus plug-in device controllers which are identical and serve the same purpose. The DHI, Model Number ADHI11, is a member of the TDC 4500 product line. The HIM, Model Number 4DP4400AE44, is a member of the HS4400 computer line. The DHI/HIM, herein will be referred to as the "interface".

2. PRECAUTIONS

When testing or repairing the interface boards, while the system is active, insure that data will not be transmitted to the hiway where such data can cause other system problems. Transmission can be disabled by removing the hiway cable from the backpanel cable adapter and installing terminators.

When removing or inserting boards or IC chips, make certain that all GENIE Bus power is turned off. When replacing memory chips, such as ROM's, PROM's, or RAM's, be sure that the chips are correctly inserted in their sockets before applying power. Check board drawing for chip to socket orientation. Note RTV adhesive is used to secure memory chips to sockets.

3. OPTIONS

The DHI/HIM includes a number of built-in selectable options to accommodate various applications, and to make it easier to test and troubleshoot. The application options are described in the General Description manual. The options implemented by jumper clip are summarized here:

J1 - 8 mc clock to sequence generator: The J1 clip is normally in and is pulled only for factory test purposes.

J2 - 8 mc clock to receiver/driver logic: The J2 clip is normally in and is pulled only for factory test purposes.

J3A - Switch Hiway external: This clip is normally in if the system includes a Hiway Traffic Director (HTD).

J3B - Switch Hiway Internal: This clip is normally in if the system does not include the HTD.

J4 - Jabbr: This clip is normally in to insure that the hiway cannot be tied-up by a run-away or noisy transmitter. The clip is pulled for test purposes only.

The device address switches, device priority switches, and all jumper clips are located on the HIDA1 board. The hiway address switches, along with the internal polling and source check switches, are all located on the HICAW (Wire Wrap) or HICA1 (copper) board.

4. REFERENCES

The following documents are either required or will be of assistance in understanding and maintaining the DHI/HIM.

- Logic

  51300734 - Hiway Interface Module

- Theory of Operation
  - ADHI-T DHI/HIM Theory
  - 4400AA10GC-T GENIE Bus and Controller Theory (HS4400)
  - ACPU1GC-T GENIE Bus and Controller Theory (TDC 4500)

- Test and Diagnostic Program

  Test Module, Rev. D System Exerciser (Factory Test) 51191039

- Interface Cables and Wiring

  51101580 - Card Edge Jumper Cable

- Microprogram Listing

  51120017 - HIM 44 Firmware

- Printed Wiring Board/Assembly
  - PX4000HIDA1 - Interface Driver Board
  - Interface Controller Board (see Section 12)
    51102516-101 – HICAW (wire-wrap)
    51102516-201 – HICA1 (copper)

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5. COMPONENT LOCATIONS

All of the DHI/HIM hardware is contained on two boards and a cable adpater. The boards occupy three adjacent card slots in the GENIE Bus chassis. The cable adapter is located on the backpanel of the same chassis and attaches to the "B" connector field of the HIDA1 board.

6. TEST EQUIPMENT AND MATERIAL

The following test equipment and materials are either required or will provide assistance in testing and troubleshooting the DHI/HIM.

- Test Module, Rev. D System Exerciser 51191050
  HIM Test Module 51191035
- MEP's PWB Extender
- Oscilloscope With Dual Trace
- General Purpose Multimeter
- BNC Terminator P/N 30732052-001 (PCKA02)

7. PREVENTIVE MAINTENANCE

There are no adjustable components associated with the DHI/HIM; therefore, no preventive maintenance schedule is provided. The interface is tested along with other members of the subsystem during initial installation and thereafter as required following replacement or other corrective maintenance.

8. PERFORMANCE TESTS

The purpose of the performance tests is to provide reasonable assurance that the DHI/HIM is operating properly and is ready for on-line system usage. These tests are normally conducted during initial installation, after major repairs (PWB replacement) and as required to isolate problems between system components and system software. Scheduled or periodic maintenance is not required.

8.1 Preliminary

The DHI/HIM PWA's are normally shipped already installed in the GENIE Bus chassis. The actual location (three card slots) is assigned at the system level. The PWA's should be removed to verify that all switching and strapping options are set per system assignment.

The allowable switch and jumper configurations are listed and illustrated on sheet 1.1 of logic drawing 51300734.

Handle PWA's carefully, component side up, and keep hands off the contact pin field areas.

After the computer is up and running, proceed as follows:

A. Check power supply voltages at the chassis backpanel. The interface requires +5 V ± 3%, +15 V ± 3%, and -15 V ± 3%. For voltage and ground pin connnections refer to logic sheet 4 for the HIDA1, and logic sheet 14 for the HICAW.

   Before performing the following checks, insure that the boards and cable adapter are properly installed and that all cables are connected, except the hiway cables. Install BNC terminators on adapter panel plugs.

B. Power Up the computer system. Note that both the Hiway "A" and "alarm" indicators light up (alarm on indicates no Bus alarm). Refer to Fig. 1 for location of indicator lamps.

C. Activate the interface by executing ACT S'=0. Note that the "activate" indicator lights up.

D. Load "A" and output all three memory parameter words to the interface buffer (RAM); then, input each word for comparison. The GEN 2 instructions and A register formats are listed in the General Description Manual.

8.2 System Test (Factory)

Connect the hiway cables and load the system test module. Stage 1 tests operate the interface in the loopback, self-test mode. Stage 2 tests require that the interface have hiway access to other TDC 2000/7100 devices, including a PIU with special test configuration in the first PCFA. Additional system test information will be provided when available.

9. ASSEMBLY AND DISASSEMBLY

All of the components associated with the DHI/HIM are contained on two printed wiring boards and an adapter panel. Many of the IC devices, such as the ROM's, PROM's and RAM's are sensitive to static electricity and may be damaged if not handled properly.

When inserting IC's in their sockets, make certain that the pin to socket orientation is correct (pin 1 to pin 1) prior to applying operating power. Note: Use RTV adhesive to secure the RAM's after testing.

10. ADJUSTMENTS

There are no adjustable components associated with the DHI/HIM logic. The backpanel power supply voltages, +5 V, +15 V, and -15 V, are furnished by the host computer power supply modules. Voltage adjustments for these power supplies are described in the system power section of the computer maintenance manual.

11. TROUBLESHOOTING

Due to the complexity of logic and memory, and the extensive test equipment requirements, it is recommended that field repairs and troubleshooting be limited to the board replacement level only. If the performance test, or system usage indicates that the DHI/HIM is not doing everything it is designed to do, the most practical and expedient thing to do is replace the boards, one at a time. Defective boards should be tagged and returned to Phoenix where they can be repaired and cycles through factory test.

12. ILLUSTRATED PARTS

All of the component parts associated with the DHI/HIM are contained on the PWA's and the cable adapter. Part numbers for these components are listed on the parts lists (PL's) associated with each assembly. Interconnecting cables and mounting hardware are shown in the computer parts manual.

Note the HICAW and HICA1 boards are interchangeable. To order, use P/N 51102516-101 or 201. This will get you a fully tested board, complete with proms.

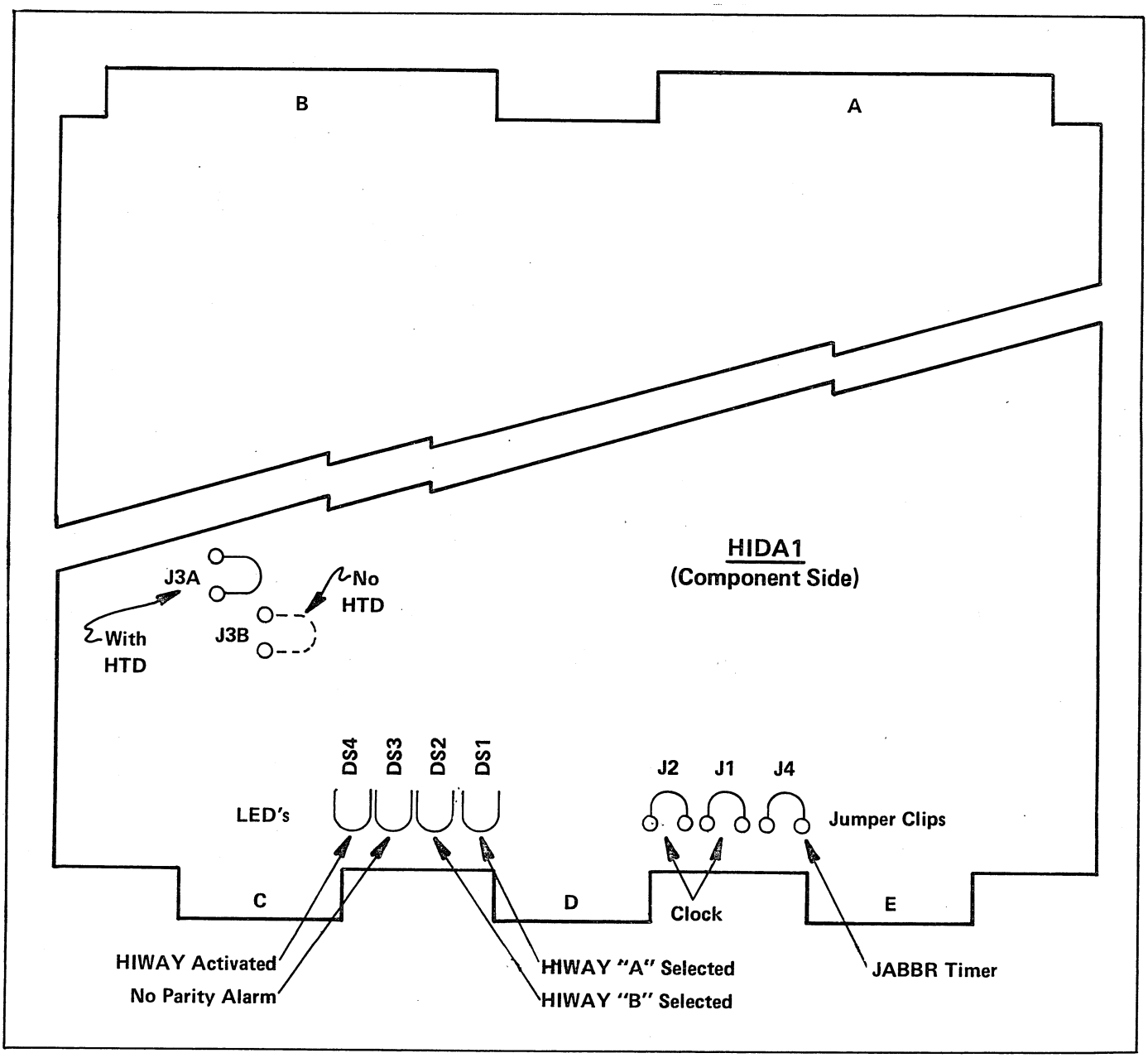

Figure 1

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